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Implementation of Area-Efficient and Low Power OFDM Architecture

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Abstract: Fast Fourier Transform (FFT) algorithm is extensively used in numerous signal processing and communication systems. Due to its rigorous computational requirements, it occupies large area and consumes high power if implemented in hardware. By using the FFT concepts we are certainly in emerging efficient architectures for wireless networks which are common in universally now-a-days. The SDC processing engine (PE) is proposed to achieve 100% hardware resource utilization by sharing the common arithmetic resource in the time-multiplexed approach, including both adders and multipliers.

Keywords: FFT, Pipelined Architecture, SDF-SDC.

I. INTRODUCTION

Wireless communication has turn out to be one of the fastest mounting markets worldwide [1]. The main reasons for this success are the emergence of low-cost end-user terminals, global standardization efforts and affordable communication services. Until the end of the 1990s, the focus has mainly been on mobile telecommunication. However, in the meantime voice-centric systems have reached a close-to 100% market proliferation in Europe, USA and in many countries of Asia. With the advent of portable computers, personal digital assistants (PDAs) and multimedia capable mobile terminals (phones), wireless data networks and services have recently attracted significant attention and are widely considered to be the market of the future. Consequently, new standards have been defined to replace today's wired data connections with radio links. Cellular data networks are thereby usually extensions of wide-area mobile telecommunication systems that provide wireless connectivity with medium data rates on a global scale to a large number of nomadic users. Wireless local loop (WLL) systems or wireless metropolitan area networks (WMAN) replace wired data connections to homes and offices. Finally, wireless local area networks (WLAN) offer wireless connectivity to computer networks with very high data rates to a small and medium number of users in office and homes or in public WLAN hot-spots. In all three fields, the evolution of standards and systems is driven by the emergence of new applications which continue to require better quality of service (QoS) and higher data rates and by the need to support a growing number of users. OFDM is spectrally efficient, carrying more data per unit of bandwidth than such services as GSM and W-CDMA. Fig.1 shows a comparison of the spectral efficiency of the leading cellular technologies and how they compare to WLAN and WiMAX. Fourth Generation technology, often referred to as the Long Term Evolution of wireless (LTE) and Ultra Mobile Broadband(UMB) for cellular devices, plans to use OFDM or OFDMA.

OFDM is a multicarrier modulation technique as shown in the Fig.2, in which several carriers are transmitted over the allocated bandwidth to carry the information from source to destination.

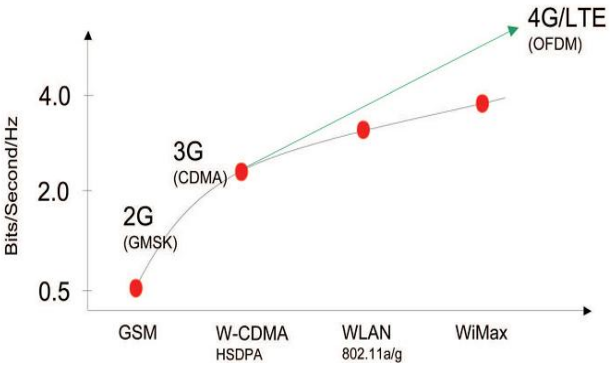

Fig. 1 Spectral efficiency of the cellular technologies

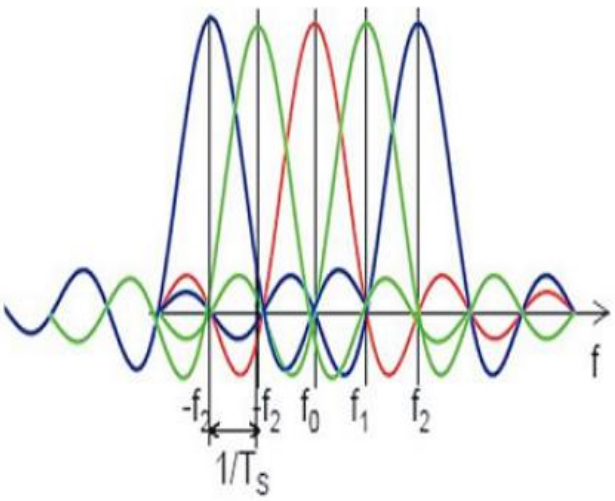

Fig. 2 OFDM Modulation

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For this, each carrier may use one of the several available digital modulation techniques like BPSK, QPSK, and QAM. The major challenge is the design of low-complexity receiver algorithms and the development of corresponding efficient VLSI architectures. Field programmable gate arrays (FPGA) are programmed specifically for the problem to be solved, hence they can achieve higher performance with lower power consumption than general purpose processors. Therefore, FPGA is a promising implementation technology for computationally intensive applications such as signal, image, and network processing tasks.

II. RELATED WORK

The custom hardware for MIMO-OFDM system based on FPGA consuming low power was designed [2].The transmitters and the receivers both were designed for Xilinx Spartan 3E and Spartan 3A FPGA devices. The design was implemented on the FPGA and experiments were performed to substantiate the design. The proposed work [2] proved that a system with very low power can be designed using FPGA device which can provide higher data rate as compared to the ordinary systems and it can be rearranged according to the condition.

In 2010, Veranna et al, [5] uses Space Time Frequency coded communication system using diversity schemes like MIMO and MISO and their performance is evaluated over a fading channel having inherent noise. MATLAB7.0.1 is used as simulation tool to compare the performance of MISO and MIMO technique. MIMO scheme performed better than MISO in comparison of BER vs. SNR. Paper also compares the channel capacity obtained by various MIMO diversities as function of signal to noise (SNR) ratio and proves that as diversity increases the channel capacity increase.

In 2013, M. Vani Divyatha et al, [4] discuss the design of MIMO-OFDM for wireless broadband communication. MIMO-OFDM is considered for different modulation schemes which are used to encode and decode the data stream in wireless communication over AWGN channel for unknown transmitter and known receiver. MIMO detection methods are investigated on VBLAST architecture. At the end of the paper, there is a slight increase in the spectral efficiency by using VBLAST architecture.

In 2013, Jitendra Kumar Daksh et al, [3] discusses several aspects in the direction of Space-time coding in MIMO-OFDM systems with multiple antennas. In this paper two space time coding techniques are discussed and brief introduction can be seen. Also this paper gives the recent work of space time coding techniques and analysis of related work. Two prevailing space-time coding techniques are Space Time Block Codes (STBC) and Space Time Trellis Codes (STTC). STBC provide diversity gain, with very low decoding complexity, whereas STTC provide both diversity and coding gain at the cost of higher decoding complexity. STBC must be concatenated with an outer code to provide coding gain. Concatenating STBC with Trellis Coded Modulation (TCM) creates a bandwidth efficient system with coding gain. This paper discusses about previous results in the direction of their survey. This result in the fact of increasing the number of antenna has better transmission performance. And also increasing the states reduces the SNR.

There are various methods which have been used for designing MIMO-OFDM system. Idea behind the high spectral efficiency of OFDM is elimination of guard bands and use of the overlapping but orthogonal subcarriers. As the number of subcarriers in the system increases, processing time required to calculate IFFT and FFT also increases which further increases the spectral efficiency of the system. By increasing the number of subcarriers and by making highly pipelined architecture for IFFT and FFT the system performance could be improved in terms of processing time. The system will consume less energy due to less data transmission time.

So therefore from above discussions every communication system must have both Transmitter and Receiver. At the Transmitter side, IFFT is used for modulating signal, which depends on the OFDM system and at the Receiver side, FFT is used for demodulating signal. The FFT/IFFT is the important modules in OFDM transceivers. From this we can say that, the most parts of OFDM systems are, IFFT can be used at the transmitter side where as Viterbi decoder can be used at the receiver side (Maharatna et al., 2004). The FFT is the second calculative huge block at the receiver section. The FFT and IFFT must be implemented such that to achieve the required throughput with the reduced area and delay. The modern OFDM transceivers requirements may lead to the implementation of special hardware, which is the critical block in the transceiver. Hence the FFT/IFFT can be implemented as a Very Large Scale Integrated circuit. In this paper we propose the pipelined implementation of Radix-2 based single delay feedback (R2SDF), Radix-2 single delay commutator (R2SDC), combined architecture is implemented in the receiver architecture of OFDM.

III.PROPOSED SYSTEM

Assuming that the input data enters the FFT circuit serially in a continuous flow, the radix-2 MDC and SDF architectures can be directly deduced according to the data flow graph in Fig.3.The radix-2 MDC architecture [7] is the most direct implementation approach of pipelined FFT, but its hardware utilization is only 50%. Compared with [6], the radix-2 SDF design [8] reduces the required memory size. However, the utilizations of adders and multipliers are still 50%. Besides the basic radix-2 architectures, various high radix pipelined FFT architectures have also been proposed to address the arithmetic resource utilization problem.

The proposed FFT architecture consists of one pre-stage, $\log_2 N$-1 SDC stages, one post-stage, one SDF stage, and one bit reverser, shown in Fig. 4(a).The pre-stage shuffles the Complex input data to a new sequence that consists of real part followed by the equivalent imaginary part, shown in Table 1.The corresponding post-stage shuffles back the new sequence to the complex format. The SDC stage t (t = 1, 2, .., $\log_2 N - 1$) contains a SDC PE, which can achieve

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100% arithmetic resource utilization of both complex adders and complex multipliers.

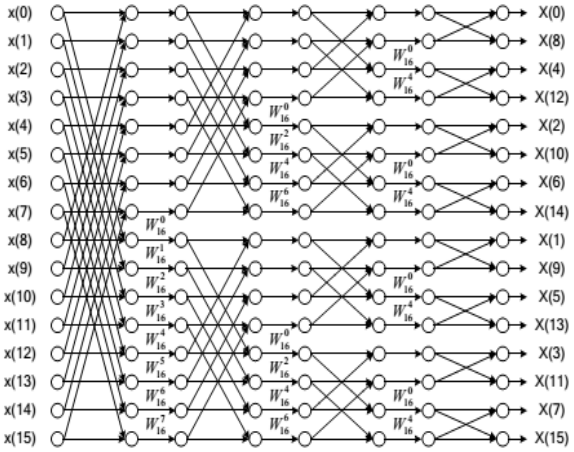

Fig.3 Data flow graph of DIF Radix-2 FFT (N = 16)

1) The SDC PE, shown in Fig. 4(b), consists of a data commutator, a real add/sub unit, and an optimum complex multiplier unit.

2) In order to minimize the arithmetic resource of the SDC PE, the most significant factor is to maximize the arithmetic resource utilization via re-ordering the data sequences of the above three units.

3) In the stage t, the data commutator shuffles its input data (Node_A) to generate a new data sequence (Node_B), whose index difference is N/2t, where t is the index of stage.

4) The new data sequence (Node_B) is critical to the real add/sub unit, where one real adder and one real subtracter can both operate on two elements for each input data.

5) The sum and difference results (Node_C) overlap the places of the two input elements. Therefore, it preserves the data sequence, requires only one realadder and one real subtracter.

6) For the optimum complex multiplier unit, its output data sequence (Node_E) should be the same as its input data sequence (Node_C).

7) If so, its output sequence (Node_E), which is also the output sequence of the SDC stage t, can become the direct input data sequence (Node_A) of the SDC stage t+1. Final, the even data are retrieved in normal order. Thus, the bit reverser requires only N/2 data buffer. The last stage of Single Delay Feedback (SDF) is identical to the radix-2 Single Delay Feedback (SDF), containing a complex adder and acomplex subtractor. By using the modified addressing method, the data with an even index are written into memory in normal order, and they are then retrieved from memory in bit-reversed order while the ones with an odd index are written in bitreversed order- Fig 5.

Normally the Fast Fourier Transform architectures are working based upon the parallel architectures, so FFT's are consume large area and latency, in order to perform low area and latency we are indeed in developing the pruning the FFT's with help of Pipelining Data path, feed forward, feed backward.

TABLE I. COMPARISON TABLE SHOWING OFDM WITH RADIX-2 BASED FFT WITH OFDM BASED OPTIMUM MULTIPLIER

	AREA (Occupied Slices)	**LUT**	**Delay (nS)**	**Frequency (MHz)**	**Power (W)**
OFDM_REC	1053	539	4.014 nS	248.128	2.772
OFDM_SDF	890	797	7.340 nS	68.120	0.295

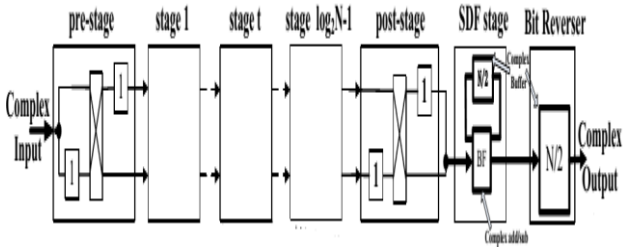

Fig.4 (a) Proposed FFT Architecture

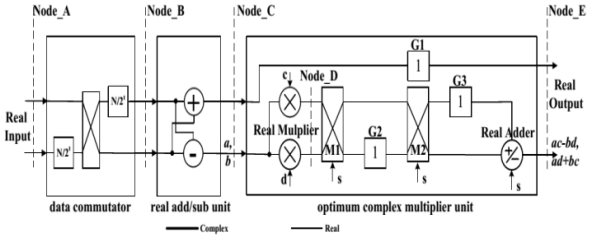

Fig.4 (b) SDC-PE of Proposed FFT Architecture

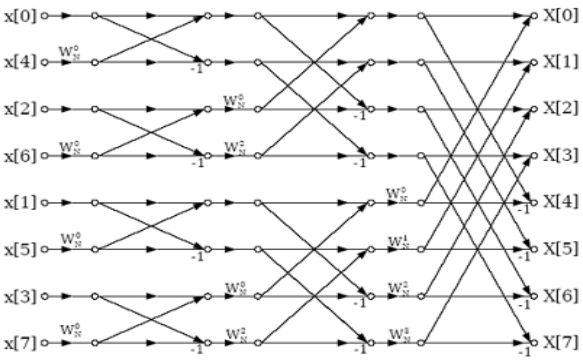

Fig. 5 Dataflow graph showing DIT based 8-point FF

The proposed system consists of the architecture that can be have the stage-1, stage-2, stage-3, stage-4, stage-5 all are designed for 64-point FFT architectures, as shown in the Fig 6.

The proposed system consists of five stages and the stage-t which is also present in 64-point FFT architecture, All FFT based architectures are Operating based upon the parallel architectures, so we are proposing a Pipelined operation of FFT radix-2 architectures with combination of SDF-SDC architectures in order to achieve higher data rate.We may observe that thisapproach requires fewer transistors than

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the other radix-2 architectures [9, 10] because of the reduction in complex multipliers.

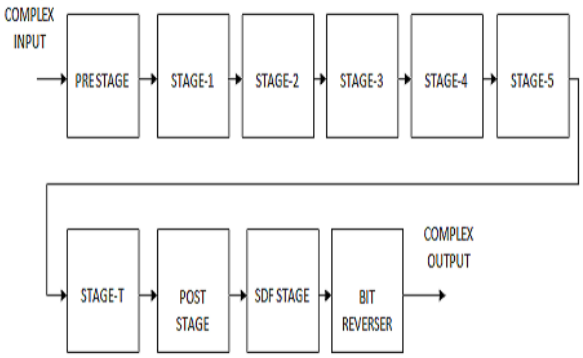

Fig.6Proposed system block diagram.

IV. CONCLUSION

The Basic architectures for FFT implementations are revealed and a contrast between the extensively approved architectures in terms of hardware complexity and choice of optimization is discussed. This Paper proposes a collective SDC-SDF pipelined FFT architecture which yields the output data in the normal order multipliers, compared with the other radix-2 FFT designs. Therefore, the proposed FFT architecture is very attractive for the single-path pipelined radix-2 FFT processors with the input and output sequences in normal order.

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BIOGRAPHIES

Rajidi Sahithi pursuing PhD in GITAM University received M.Tech degree from JNTU Hyderabad in VLSI SYSTEM DESIGN in 2010 and 2012. She is currently working as Asst.Professor indepartment of Electronics and Communication Engineering, Malla Reddy Engineering College for Women, JNTU Hyderabad and has 7 years of teaching experience. Her research interests include High Data Rate Transmissions and MIMO based OFDM Systems.

T. Venkata Ramana, as a diligent scholar has excelled instudies from his child hood. His dare to dream, to work smart and strive for nothing less than excellence and to enjoy the journey every step of the way made him to scale greater heights. He has obtained his Bachelor's Degree in Electronics & Communications Engineering from Nagarjuna University. He has completed her Masters in Systems and Control Engineering from Osmania University. He has completed his Doctoral program Ph.D. in the area Satellite Communications from the Andhra University. He took up academic pursuit and served in an array of designations like Associate Professor& Coordinator for M.Tech (Evening programs) of GITAM University. He also involved himself in teaching and research tasks. Above all he took up a mission to ignite the young minds so as to nurture the students with the potential to reach greater horizons. He strongly believed in himself, his mentors and peers and partners.

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